A study of gate stack reliability in GaN HEMTs using low frequency noise measurements

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MURI Review Meeting

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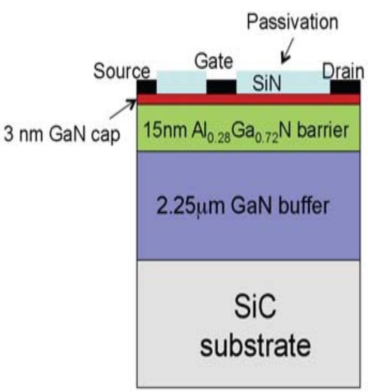
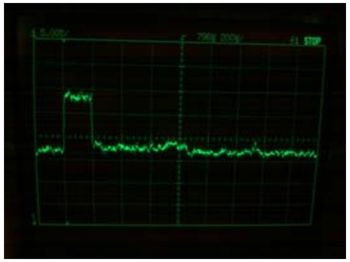
GATOR Engineering

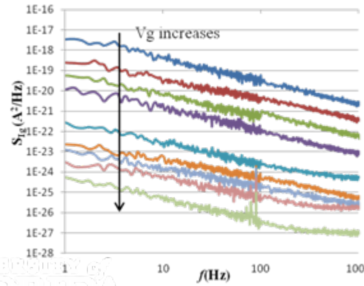
UNIVERSITY OF FLORIDA

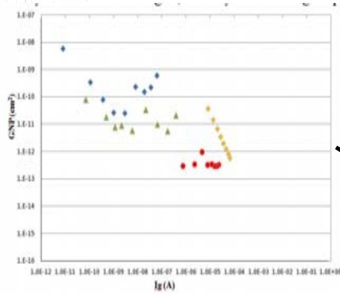
FLOORS



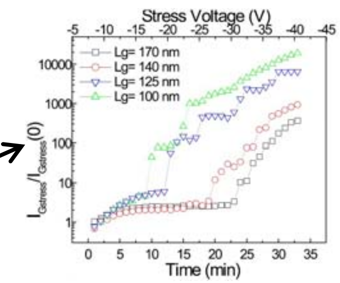
AFRL device



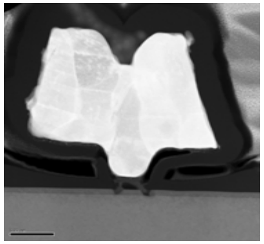




Noise Measurement



Off-state Stress (Ren Group)
Optical Pumping (David)
RF Stress （Erica)



TEM imaging (Ray)

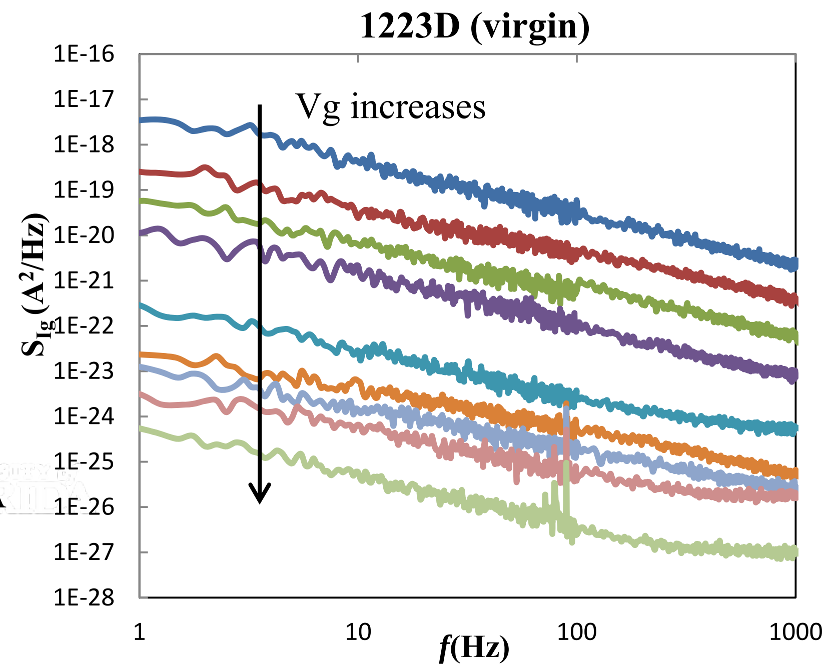
t=0, As Built

t>0, Degradation

Outline

- Gate noise parameters
- RTS noise in gate stacks
- Drain noise model
- Conclusions

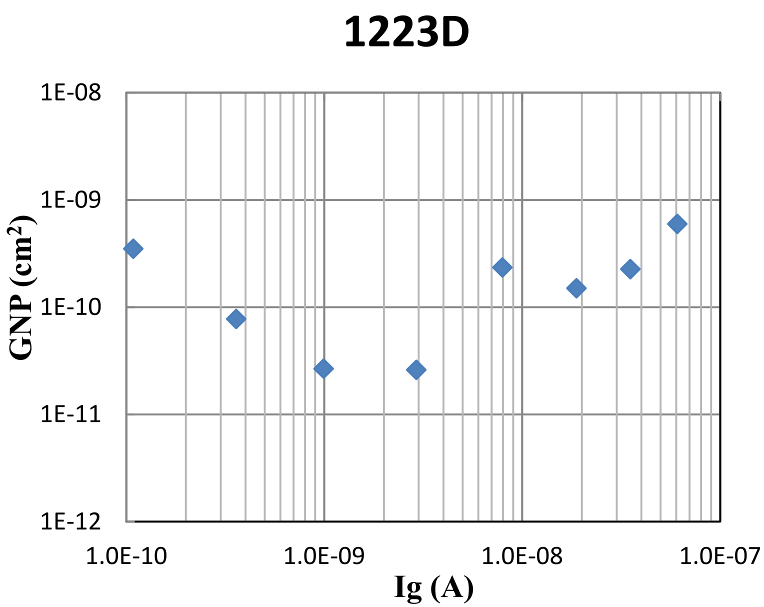
Gate Noise Measurement Setup



Source and drain were grounded.

1/f noise was measured when gate biased from -4.5V to -0.5V with 0.5V step.

GNP(Gate Noise Parameter)



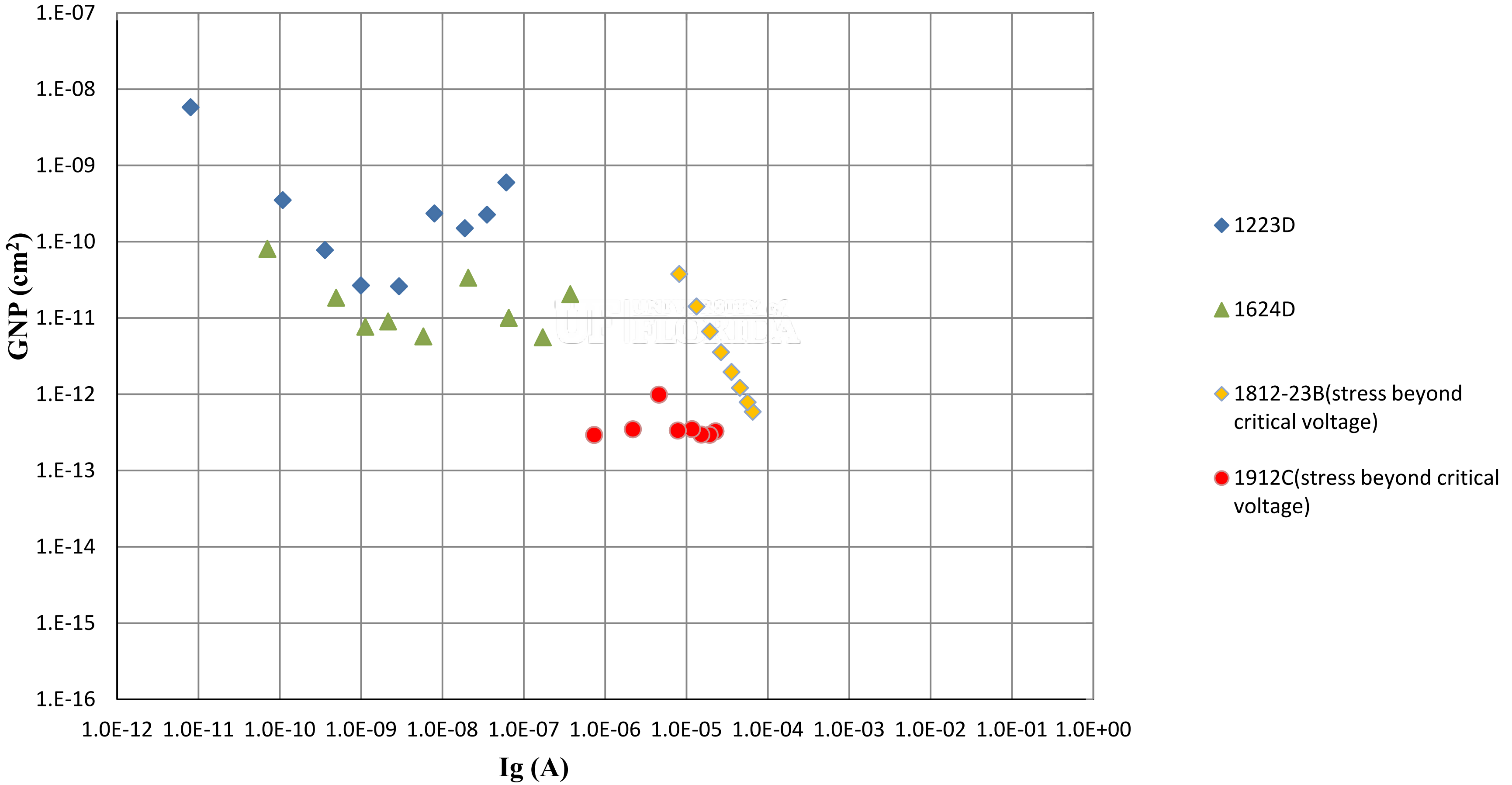
GNP (Gate Noise Parameter) is defined as

$$GNP \equiv \frac{S_{I_G} fA}{I_G^2}$$

- A figure of merit for the quality of the gate stack
- GNP is independent of gate area and bias point in the case of a uniform energy distribution of traps.
- Typical value of GNP for Silicon MOSFET is around 10^{-16} cm^2

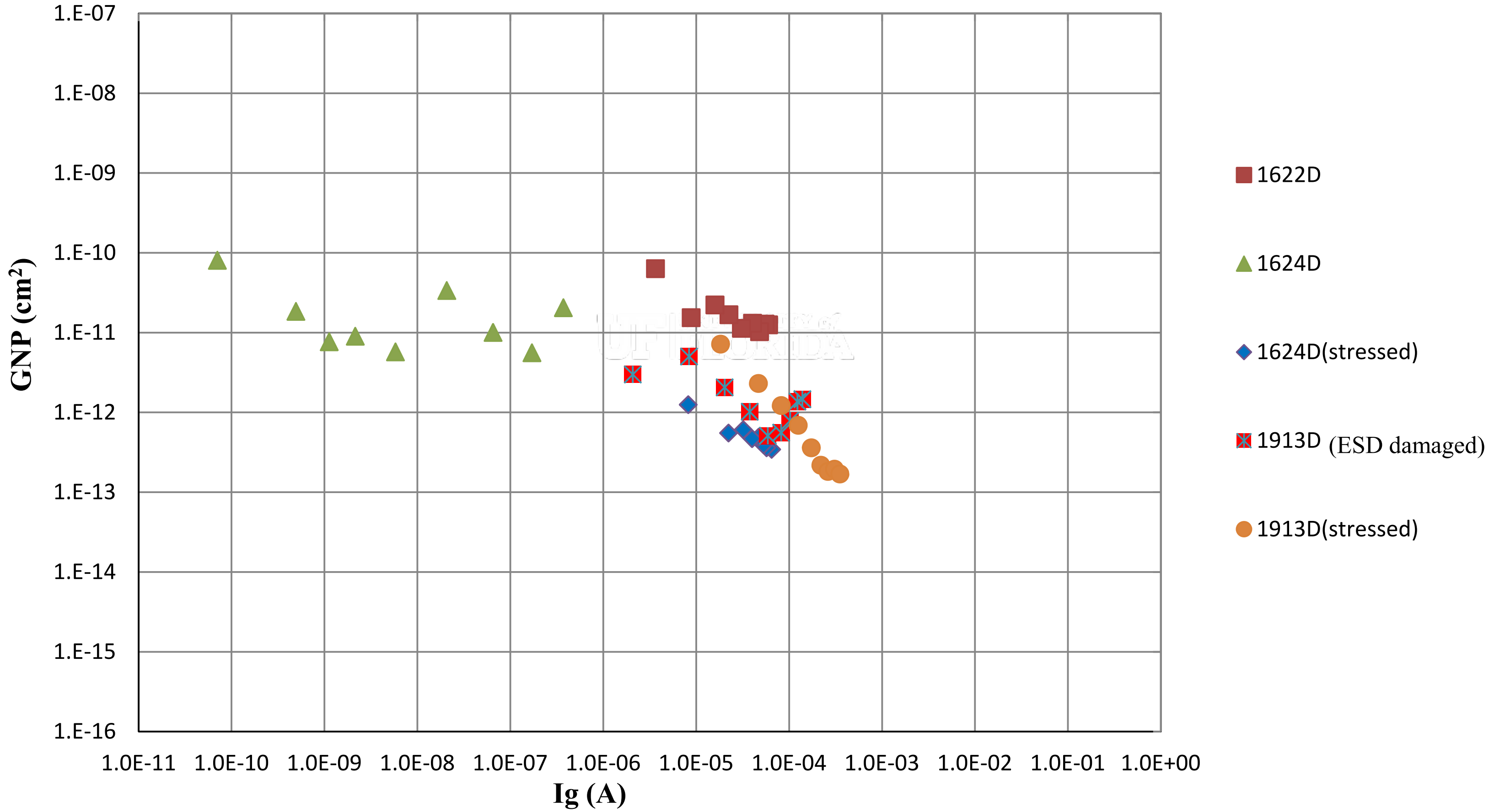
GNP of AFRL device

- AFRL virgin devices(from David) and devices after stress beyond critical voltage (done by Dr.Ren’s group)



GNP of AFRL device

AFRL devices damaged by ESD and current pulse (stressed).



Comparison of GNP

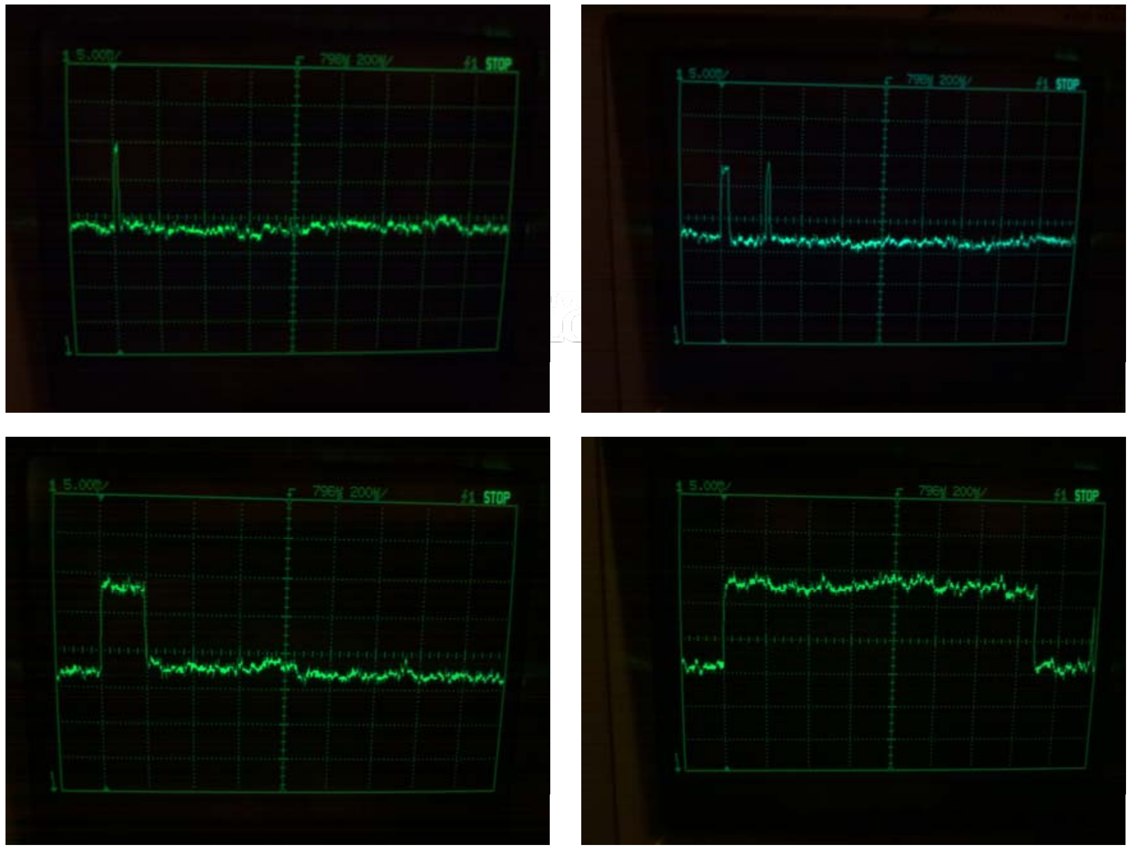
- AFRL, Commercial Device, Si MOSFET

Device	Condition	Jg(A/cm^2)	GNP(cm^2)
AFRL	Virgin	0.1~1	10^{-10} ~10^{-11}
AFRL	Off-state stress beyond Vcrit	1~100	10^{-11} ~10^{-13}
AFRL	ESD damage	1~100	10^{-11} ~10^{-12}
Commercial GaN HEMT		0.1~1	10^{-7} ~10^{-9}
Si MOSFET	SiO_2 gate stack		10^{-17} ~10^{-16}
Si MOSFET	SiON gate stack		~10^{-16}
Si MOSFET	High-K gate stack		10^{-11} ~10^{-15}

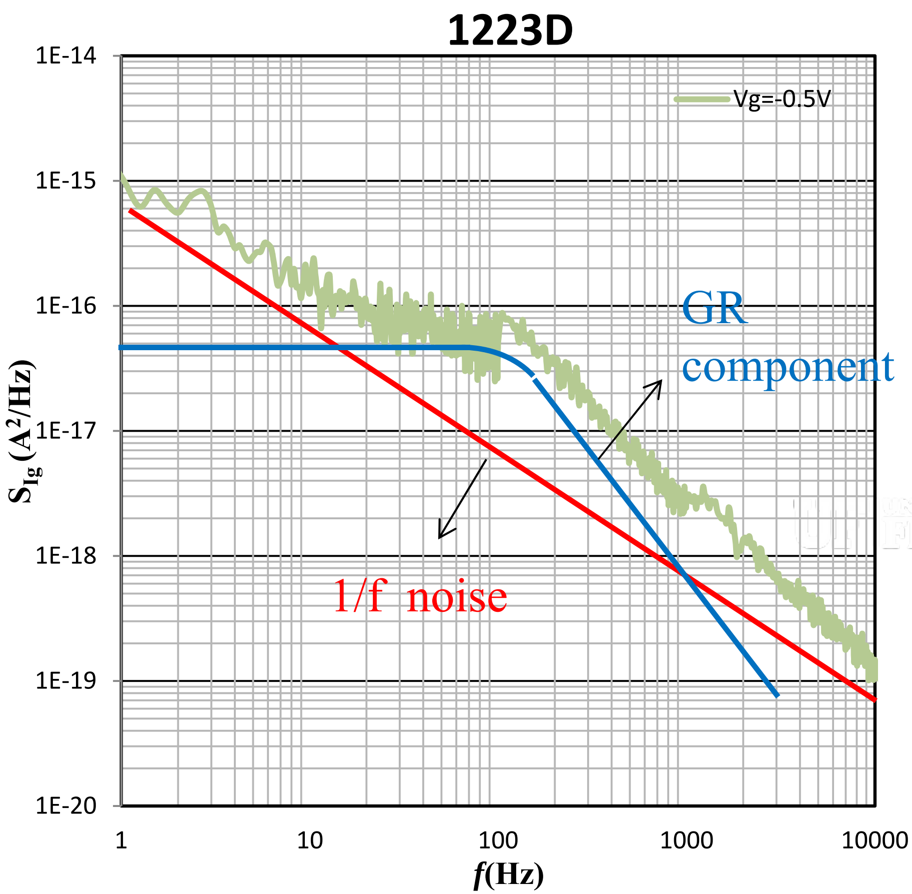
GNP of AFRL GaN HEMTs is about 2 orders lower than commercial GaN HEMTs.

RTS

- RTS (Random telegraph signal) was observed in one device (1622D) at low leakage current.



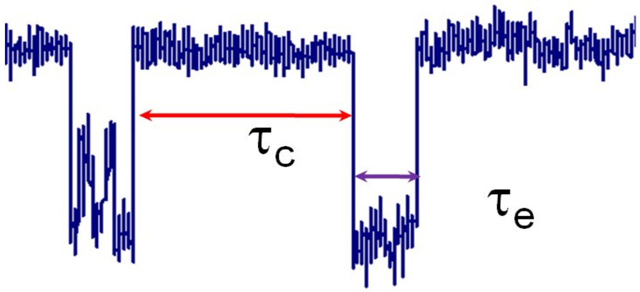
RTS and Lorentzian



$$S_{I_G}(f) = S_{1/f}(f) + \sum S_{GR}(f)$$

- Background 1/f noise.
- Lorentzian components on top indicate a trap related mechanism in the gate stack.
- Characteristic frequency of the Lorentzian is around 300Hz.

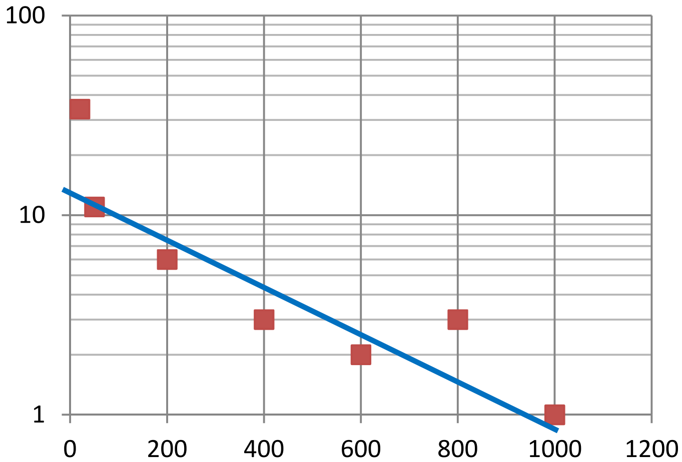
Characteristic frequency of RTS



$$\frac{\Delta I_G}{I_G} \approx 33\%$$

$$\frac{1}{\tau} = \frac{1}{\tau_c} + \frac{1}{\tau_e}$$

The capture and emission times are in accordance with Poisson distribution.



$$Count(N) = \frac{c}{\tau}\exp\left(\frac{-t}{\tau}\right)$$

$$\tau_c = 480\mu s$$

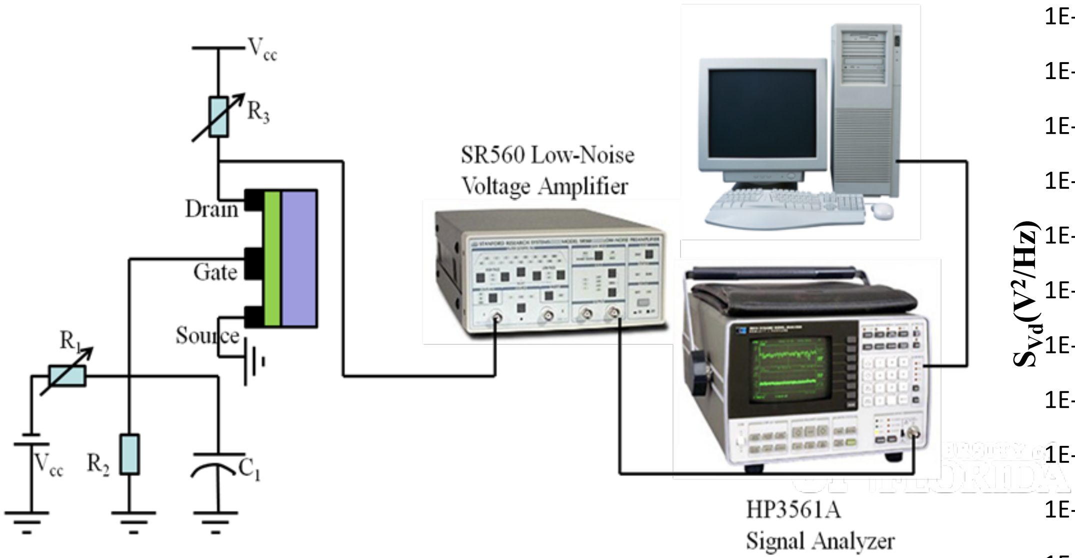
In our case τ_c is smaller than τ_e

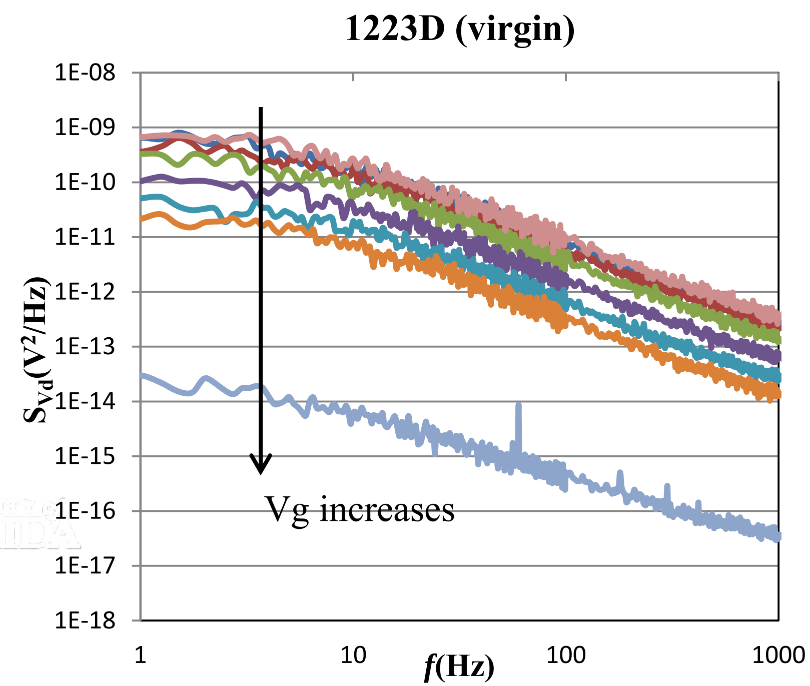
$$\tau \approx \tau_c = 480\mu s$$

Characteristic frequency

$$f = \frac{1}{2\pi \cdot \tau} \approx 300Hz$$ in accordance with noise spectrum

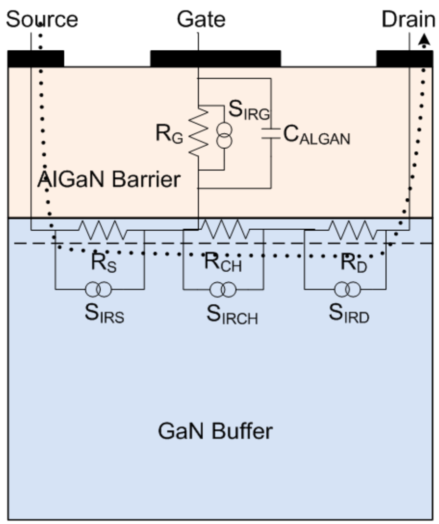
Drain Noise Measurement Setup





Keep V_{ds}=100mV during the measurement. V_{gs} bias ranges from V_T (~-3.6V)to -1V.

Series Resistances

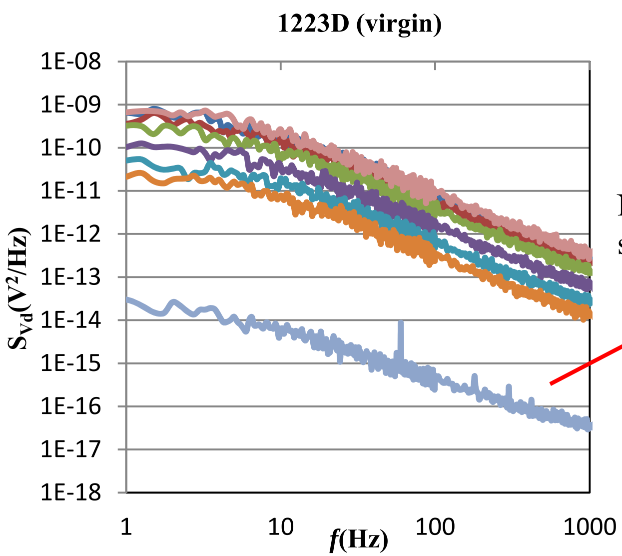


$$\frac{S_{V_d}}{V_{ds}^2} = \frac{S_{V_{Ch}}}{V_{CH}^2}\left(\frac{V_{CH}^2}{V_{ds}^2}\right) + \frac{S_{V_{SR}}}{V_{SR}^2}\left(\frac{V_{SR}^2}{V_{ds}^2}\right) = \frac{S_{I_{Ch}}}{I_{CH}^2}\left(\frac{V_{CH}^2}{V_{ds}^2}\right) + \frac{S_{I_{SR}}}{I_{SR}^2}\left(\frac{V_{SR}^2}{V_{ds}^2}\right)$$

$$\frac{S_{V_d}}{V_{ds}^2} = \frac{S_{I_{ch}} V_{CH}^2}{I_{ds}^2 V_{ds}^2} + \frac{S_{I_{SR}} V_{SR}^2}{I_{ds}^2 V_{ds}^2}$$

When V_{gs} is larger than V_T

$$\frac{S_{V_d}}{V_{ds}^2} \cong \frac{S_{I_{SR}} V_{SR}^2}{I_{ds}^2 V_{ds}^2} \cong \frac{S_{V_{SR}}}{V_{ds}^2}$$



Noise mainly from series resistances

Then we can calculate noise component from series resistances under different gate bias and extract information for the gated part of channel.

1/*f* Noise Model Of Channel Noise

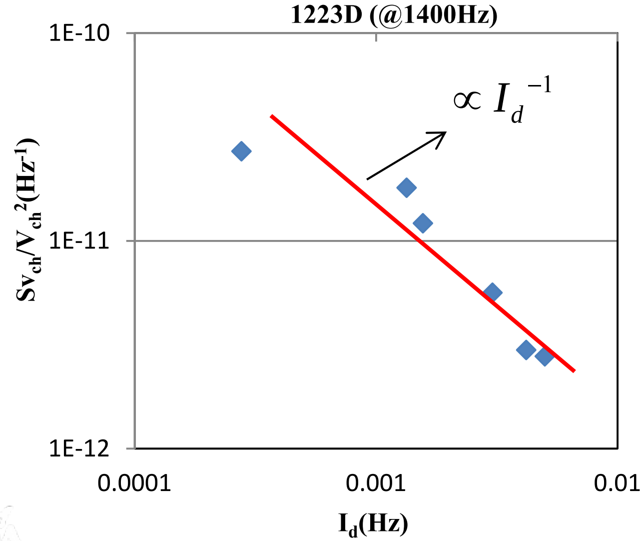
- Hooge mobility fluctuations

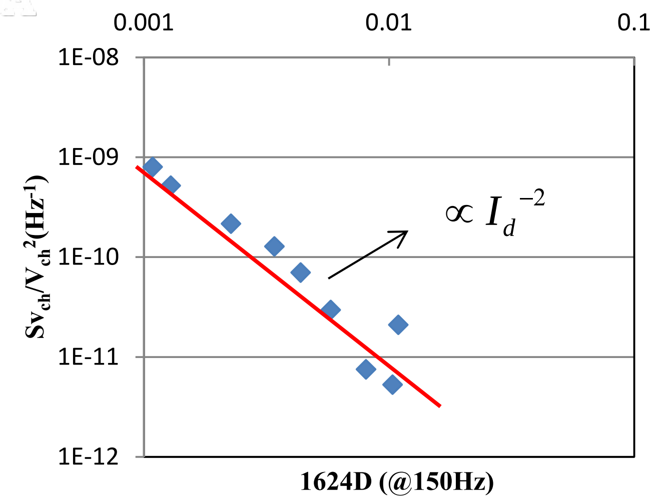
$$S_{V_{ch}} / I_{ch}^2 = \frac{\alpha_H}{Nf} \propto I_d^{\ -1}$$

- Carrier number fluctuations

$$S_{V_{ch}} / V_{ch}^2 \propto (\frac{1}{N})^2 \propto I_d^{\ -2}$$

For virgin device mobility fluctuations dominate. Carrier number fluctuations dominate on stressed device.





Hooge Parameter On Channel

For Hooge mobility fluctuations,

$$\alpha_{CH} = \frac{S_{V_{CH}} N_{CH} f}{V_{CH}^2} \qquad Where, N_{CH} = C_{AlGaN}(V_{GS} - V_T)$$

For carrier number fluctuations,

$$N_t = \frac{S_{I_d} C_{OX}^2 WLf^{\gamma}(V_{GS} - V_T)^2}{q^2 kTI_D^2 \lambda}$$

Device	Condition	α	Nt($cm^{-3}.eV^{-1}$)
AFRL	Virgin	10^{-3}	
AFRL	Off-state stress beyond Vcrit	10^{-1}	10^{21}
Commercial GaN HEMT		10^{-3}	
Si MOSFET	SiO_2 gate stack	$10^{-7} \sim 10^{-3}$	
Si MOSFET	SiON gate stack		$10^{17} \sim 10^{18}$
Si MOSFET	High-K gate stack		$10^{18} \sim 10^{20}$

Conclusions

- GNP as a figure of merit for gate stack quality was extracted from AFRL devices under different conditions.
- GNP of AFRL virgin device is about 10^{-11}, which is comparable with high-k Si MOSFET and significant lower than commercial GaN HEMTs.
- RTS in the gate noise was observed on oscilloscope under small gate bias in some devices. Time constant of RTS agrees with the reciprocal characteristic frequency of related noise spectrum.
- We establish a drain noise model to extract α and Nt to estimate channel quality. α of AFRL virgin device is about 10^{-3}.

Thank you!